high if a ZERO is received. This same operation will occur in NAND gates **332**, **334**, **336** and **338** during the next decimal digits or during the four subsequent time periods associated with decimal digit pulses CP2, CP3, CP4, CP5. Thus, if a ZERO is received and consequently the outputs of any one of the NAND gates **330** through **338** goes low, the output of a common NAND gate **340** goes high. Conversely, if a ONE is received, the outputs of all of the NAND gates **330** through **338** remain high and the output of common NAND gate **340** remains low. The output of this common NAND gate **340** is fed as one input to an EXCLUSIVE OR logic circuit including NAND gates **342**, **344** and **346**. When a ONE or high signal is received from the buffer storage **124** by one input of NAND gate **342**, and the other input to the NAND gate **342** from common NAND gate **340** is high because a ONE was received from the data digit storage **126**, the output of NAND gate **342** goes low. This low output is fed to the NAND gate **344** along with the ONE (high) signal from the buffer storage **124**, whereupon the output of NAND gate **344** goes high. The low output of NAND gate **342** is also fed to an input of NAND gate **346** and the high output of common NAND gate **340** is fed to the other input of NAND gate **346**, causing its output to go high. These signals are fed to the common NAND gate **328** such that the output of NAND gate **328** remains low when all of the inputs to it are high. Thus, if the output from NAND gate **328** is low, the signal is at a data verified level.

If, however, the data from the data digit storage **126** and from the buffer storage **124** do not correspond, at least one of the outputs from the EXCLUSIVE OR logic to the common NAND gate **328** goes low, whereupon the output from the common NAND gate will go high, thereby producing a data not-verified level in the verify signal.

This verify signal is fed to the data verify circuit **158**, illustrated in FIG. *6a*, which generates an output signal only when the data is verified to turn on the digital display **136**. In operation, when a data verify signal is received from the EXCLUSIVE OR circuit, it will either be low if the data is verified, or high if the data is not verified. Considering the data verified condition first, the low data verified signal from the EXCLUSIVE OR circuit of FIG. **11** and the high CLOCKED TRANSFER pulses at the end of each word are received at the inputs of NAND gate **350** causing its output to go high. This high output and the normally high POWER ON-CLEAR signal from the power on clear circuit **157** are received at the inputs of NAND gate **352**, resulting in a low NAND output. During all five data words, this low output is received at the J input of a J-K flip-flop **354**, while the K input receives the normally low CPJ signal from the transfer generator **132** of FIG. **9**. As a result, the J-K flip-flop does not switch and the $\overline{Q}$ output remains high. At the end of the comparison, that is, after word **5**, this $\overline{Q}$ output and the high CPJ signal are received at the inputs of NAND gate **356** resulting in a low output. This low NAND output and the signal from the multivibrator circuit **156** are received at the inputs of NAND gate **358** resulting in a high output. This high NAND output is received at the J input of a J-K flip-flop **360**, with the K input thereof connected to ground. As a result, the Q output of **360** goes high, and the $\overline{Q}$ output goes low, enabling power to the displays through logic switching block **370**. Flip-flop **360** is cleared initially by a $\overline{\text{CLEAR}}$ pulse generated in circuit **156**.

Considering now the condition when the data is not verified, the data verify signal is high. This high data verify signal is received at one input of NAND gate **350**, while the other input receives the high CLOCKED TRANSFER pulse at the end of each word. As a result, the output of NAND gate **350** goes low. This low NAND output signal and the normally high POWER ON-CLEAR signal are received at the inputs of NAND gate **352**, causing the output thereof to go high. This high NAND output is received at the J input of J-K flip-flop **354**, causing the flip-flop to be set and the $\overline{Q}$ output to go high and the Q output to go low. At CPJ time, the low $\overline{Q}$ signal of flip-flop **354** is presented at the J input to flip-flop **360** through NAND gates **356** and **358** and flip-flop **360** Q output remains low. CPJ time is also presented to the K input of flip-flop **354**, causing the Q output to go low at the next clock time in preparation for the next label scan. If all words are verified, the J-K flip-flop **354** will not be switched from the state established one clock time after CPJ time. In other words, flip-flop **354** remains reset through the entire verification process if no error is detected, thus allowing flip-flop **360** to be set at CPJ time.

Therefore, when the data is verified, the low $\overline{Q}$ output of J-K flip-flop **360** is fed to a relay circuit **370** which closes a circuit to one side of the lamps in the digital display **136** since, as previously stated, the digital display **136** can include a binary to decimal encoder having ten outputs, each of which is associated with a separate digit, 0 through 9, of the decimal system. Thus, this one out of ten decimal output will complete the circuit to one out of the ten lamps, so that that particular number can be displayed.

The $\overline{Q}$ output of flip-flop **360** and the Q output of flip-flop **284** in the preamble recognize circuit **128** of FIG. **9** are fed through a NAND gate **372** to enable the generation of CP1 through CP5.

While the salient features have been illustrated and described with respect to a particular embodiment, it should be readily apparent that modifications can be made within the spirit and scope of the invention, and it is therefore not desired to limit the invention to the exact details shown and described.

We claim:

1. An apparatus for reading a coded information medium having a plurality of spaced multibit words in a sequence of lines which produce coded information pulses of either a first level of response or a second level of response comprising:

a reader operably coupled to sequentially scan the spaced multibit words of the medium for detecting energy therefrom in the form of an elongate cross section progressing in a different incremental radial direction throughout 360° of rotation on each sequential scan for producing in response to the levels of energy detected therefrom a plurality of spaced words of coded information pulses corresponding to information on the coded medium only when the scan occurs at substantially a predetermined angle across the medium;

sampler means coupled to receive the coded information pulses of each word for sampling a narrow portion within the coded information pulse durations at a predetermined rate; and

a pulse processor means including a synchronizer means coupled to said sampler means and coupled to receive the coded information pulses for resynchronizing the sampling operation of said sampler for each word in response to a portion of predetermined coded information pulse signal characteristics associated with a fixed position relative to each word.

2. In the circuit of claim 1 in which the portion of predetermined coded information pulse signal characteristics is located at the beginning of each word of coded information pulses, and said synchronizer means coupled to said sampler means and coupled to receive the coded information pulses for resynchronizing the sampling operation of said sampler means in response to each portion of predetermined coded information pulse signal characteristics received.

3. In the circuit of claim 2, in which said synchronizer means is responsive to coded information pulses from a portion of the medium which produces one level of response for a duration sufficient to synchronize said synchronizer means before receiving coded information pulses associated with a unique preamble word, said pulse processor further including recognizer means coupled to receive the coded information pulses associated with the unique preamble word for enabling said pulse processor to process data word coded information pulses only after the unique preamble word is recognized.

4. In the circuit of claim 1 in which said synchronizer means is responsive to the portion of predetermined coded information pulse signal characteristics located at the beginning of